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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,075	08/20/2004	Gary D. Grise	BUR920040061US1	5074

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,075	GRISE ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-42* is/are pending in the application.

4a) Of the above claim(s) *1-24 and 43-70* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25,27,34 and 36* is/are rejected.

7)☒ Claim(s) *26,28-33,35 and 37-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Restriction Requirement mailed on 10/03/2006, Applicant has provisionally elected Group II, claims 25-42. Therefore, claims 25-42 have been examined. Claims 1-24 and 43-70 are withdrawn from consideration.

Election/Restrictions

2. Applicant's election with traverse of elected Group II, claims 25-42, in the reply filed on 10/26/2006 is acknowledged. The traversal is on the ground(s) that the subject matter of all claims 1-70 is sufficiently related that a thorough search for the subject matter of any one group of claims would encompass a search for the subject matter of the remaining claims. This is not found persuasive because of the reasons set forth in the Restriction Requirement of 10/03/2006 on pages 3-6.

The requirement is still deemed proper and is therefore made FINAL.

3. The Applicants' are reminded that in order to expedite the prosecution for the subject application, **the non-elected claims should be canceled in response to this office action**.

Claim Objections

4. The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

Claims 25-42 objected to for containing a plurality of elements or steps which are not separated by a line indent. An amendment is required to put the claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements.

5. Claim 28 is objected to because of the following informalities: the limitation, "generate a first B clock pulse" and "followed by a C clock pulse" does not show which pin it is related to. These limitations should be changed to recite: "generate a first B clock pulse on said ZB clock output" and "followed by a C clock pulse on said ZC clock output". Appropriate correction is required.

6. Claim 37 is objected to because of the following informalities: the phrase "generating a first B clock pulse" and "followed by a C clock pulse" does not show which pin it is related to. These limitations should be changed to recite: "generating a first B clock pulse on said ZB clock output" and "followed by a C clock pulse on said ZC clock output". Appropriate correction is required.

7. Claims 26, 28-33, 35 and 37-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, the claim objections to claims 28 and 37 above must be corrected before they would be allowed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 25, 27, 34 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Lackey (US-6467044), hereinafter Lackey.

Claims 25 and 34:

Lackey teaches a test controller (**The clock templates 12 are designed for use in a test controller, Fig. 1, col. 3, ll. 36-37**) having a test input connected to said test pin, a first test clock input (**B**) connected to said first test clock pin, a functional clock input connected to said functional clock pin (**oscillator 10 generates system clock, Fig. 1, col. 3, ll. 33-34**), a first control output and a second control output. Lackey also teaches a clock splitter (**clock splitter 50, Fig. 3 and Fig. 5, col. 4, ll. 40-60**) having a first clock input (**C clock, Fig. 5**) connected to said second test clock pin, a second clock input connected to said functional clock pin (**System clock, Fig. 5**), a first control input (**Y clock, Fig. 5**) connected to said first control output of said test controller, a second control input (**B clock, Fig. 5**) connected to said second control output and of said controller, an enable input (**LSSD MODE bar, Fig. 5**) connected to said enable pin, a ZB clock output (**Bout, Fig. 5**) and a ZC clock output (**Cout, Fig. 5**). Lackey also teaches an LSSD scan chain (**LSSD latches 52,54 and 56,58, Fig. 3**) comprised of

serially connected latches, a first stage of each latch having an first data input (**Data In**), a second data input and a C clock input connected to said ZC clock output of said clock splitter (**Capture Clock**), an A CLK input connected to said third test clock pin, a second stage of each latch having a data output and a B clock input connected to said ZB clock output of said clock splitter (**Launch Clock**), a data output of a previous latch connected to a first input pin of an immediately subsequent latch, a first data input of a first latch of said LSSD scan chain connected to said scan-in pin and a data output pin of a last scan chain latch of said scan chain connected to said scan-out pin.

Claims 27 and 36:

Lackey teaches additional clock splitters (**clock splitters 30, 32 and 34, Fig. 1**) connected to said test controller, some or all of said additional clock splitters connected to corresponding additional scan chains.

Allowable Subject Matter

9. Claims 26, 28-33, 35 and 37-42 are allowed. **See claim objection for these claims.**

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to the field of integrated circuit testing; more specifically, it relates to a circuit and method for testing integrated circuits at functional frequency.

The claimed invention as set forth in **claims 26** and **35** recite features such as: a test controller that includes:

an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;

combinational logic coupled to said first, second and third latches, said combinational logic coupled to said test pin, said first test clock pin and said functional clock pin;

said first latch coupled through said combinational logic to said second control output; and

said feedback connection of said second latch further coupled through said combinational logic to said first control output.

The prior arts of record teach a test controller (**The clock templates 12 are designed for use in a test controller, Fig. 1, col. 3, ll. 36-37**) having a test input connected to said test pin, a first test clock input (**B**) connected to said first test clock pin, a functional clock input connected to said functional clock pin (**oscillator 10 generates system clock, Fig. 1, col. 3, ll. 33-34**), a first control output and a second control output; Lackey (US-6467044) is one example of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, the detailed structure of the test controller of **claims 26** and **35**. As such, modification of the prior art of record to include the claimed *test controller* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the

invention would have made the necessary modifications to the prior art of record to encompass the *test controller* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *test controller* as set forth in **claims 26** and **35**.

The claimed invention as set forth in **claims 28** and **37** recite features such as:

said test controller is responsive to generate a first control signal having a duration of one cycle of said functional clock signal on said first control pin and to generate a second control signal having a duration of two cycles of said functional clock signal on said second control output upon a transition from a first state to a second state of a test signal applied to said test pin, said first control signal starting a half cycle of said functional clock cycle after the start of said second control signal; and

said clock splitter is responsive to generate a first B clock pulse, followed by a C clock pulse, followed by a second B clock pulse, said B and C clock pulses at the same frequency as said functional clock signal, based on said first and second control signals.

The prior arts of record teach test controller 12 is responsive to the System clock and a clock splitter 50 responsive to generate a B clock pulse and a C clock pulse; Lackey (US-6467044) is one example of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, the control and clock signals generated by the test controller and clock splitter as claimed. As such, modification of the prior art of record to include the claimed *control and clock signals generated by the test controller and clock splitter* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art

themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *control and clock signals generated by the test controller and clock splitter* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *control and clock signals generated by the test controller and clock splitter* as set forth in claim **claims 28** and **37**.

Hence, claims 26, 28-33, 35 and 37-42 are allowable over the prior arts of record. **Again, see claim objection for these claims.**

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Flanagan et al. (US-7058866).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 12/13/06

John J. Tabone, Jr.
Examiner
Art Unit 2138

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SUPERVISORY PATENT EXAMINER
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